EUROPEAN PATENT OFFICE
U.S. PATENT AND TRADEMARK OFFICE

CPC NOTICE OF CHANGES 1039

DATE: FEBRUARY 1, 2021

PROJECT MP0483

Action	**Subclass**	**Group(s)**
SCHEME:		
Titles Changed:	G11C	Subclass
	G11C	5/00, 5/005, 5/14, 5/141, 5/142, 5/143, 5/145, 5/146, 5/147
	G11C	7/00, 7/06, 7/1069, 7/20
	G11C	8/00, 8/04, 8/06, 8/12, 8/16, 8/20
	G11C	11/02, 11/04, 11/06035, 11/06078, 11/08, 11/16, 11/20, 11/22, 11/23, 11/26, 11/265, 11/28, 11/30, 11/34, 11/35, 11/4072, 11/412, 11/4125, 11/413, 11/42, 11/44, 11/50, 11/56
	G11C	13/00, 13/02, 13/04, 13/042, 13/06
	G11C	14/00
	G11C	15/00
	G11C	16/02, 16/0458, 16/0475, 16/06
	G11C	17/00, 17/18
	G11C	19/00, 19/08, 19/085, 19/0866, 19/0875, 19/0883, 19/188, 19/28, 19/287, 19/30, 19/32, 19/34
	G11C	21/005, 21/02
	G11C	23/00
	G11C	25/00
	G11C	27/00, 27/02, 27/04
	G11C	29/00, 29/006, 29/48, 29/787, 29/789
Notes Modified:	G11C	Subclass
DEFINITIONS:		
Definitions New:	G11C	5/005, 5/14, 5/141, 5/142, 5/145, 5/146, 5/147
		7/06, 7/1069
		8/06
		11/04, 11/08, 11/20, 11/23, 11/26, 11/265, 11/28, 11/30, 11/35, 11/4125, 11/50
		13/04, 13/042
		16/0458, 16/0475
		19/08, 19/085, 19/0866, 19/0875, 19/0883, 19/188, 19/287, 19/34
		21/005, 21/02
		27/02, 27/04
		29/006, 29/48
Definitions Modified:	G11C	Subclass
	G11C	5/00, 5/143
	G11C	7/00
		8/00, 8/04, 8/16
		11/00, 11/16, 11/22, 11/56
		13/00, 13/02, 13/06
		14/00
		15/00

CPC NOTICE OF CHANGES 1039

DATE: FEBRUARY 1, 2021

PROJECT MP0483

Action	**Subclass**	**Group(s)**
		16/00
		17/00
		19/00
		23/00
		25/00
		27/00
		29/00

The following classification changes will be effected by this Notice of Changes:

This Notice of Changes includes the following *[Check the ones included]:*

1. CLASSIFICATION SCHEME CHANGES
   - ☒ A. New, Modified or Deleted Group(s)
   - ☐ B. New, Modified or Deleted Warning(s)
   - ☒ C. New, Modified or Deleted Note(s)
   - ☐ D. New, Modified or Deleted Guidance Heading(s)
2. DEFINITIONS
   - ☒ A. New or Modified Definitions (Full definition template)
   - ☒ B. Modified or Deleted Definitions (Definitions Quick Fix)
3. ☐ REVISION CONCORDANCE LIST (RCL)
4. ☐ CHANGES TO THE CPC-TO-IPC CONCORDANCE LIST (CICL)
5. ☐ CHANGES TO THE CROSS-REFERENCE LIST (CRL)

CPC NOTICE OF CHANGES 1039

DATE: FEBRUARY 1, 2021

PROJECT MP0483

1. CLASSIFICATION SCHEME CHANGES

A. New, Modified or Deleted Group(s)

SUBCLASS G11C – STATIC STORES

Type*	**Symbol**	**Indent Level Number of dots (e.g. 0, 1, 2)**	**Title "CPC only" text should normally be enclosed in {curly brackets}****	**Transferred to#**
M	G11C	Subclass	STATIC STORES (semiconductor devices for storage H01L, e.g. H01L 27/108 – H01L 27/11597)	
M	G11C 5/00	0	Details of stores covered by group G11C 11/00	
M	G11C 5/005	1	{Circuit means for protection against loss of information of semiconductor storage devices}	
M	G11C 5/14	1	Power supply arrangements {, e.g. power down, chip selection or deselection, layout of wirings or power grids, or multiple supply levels}	
M	G11C 5/141	2	{Battery and back-up supplies}	
M	G11C 5/142	2	{Contactless power supplies, e.g. RF, induction, or IR}	
M	G11C 5/143	2	{Detection of memory cassette insertion or removal; Continuity checks of supply or ground lines; Detection of supply variations, interruptions or levels (G11C 5/148 takes precedence); Switching between alternative supplies (G11C 5/141 takes precedence)}	
M	G11C 5/145	2	{Applications of charge pumps; Boosted voltage circuits; Clamp circuits therefor (G11C 5/141 takes precedence)}	
M	G11C 5/146	3	{Substrate bias generators (G11C 5/141 takes precedence)}	
M	G11C 5/147	2	{Voltage reference generators, voltage or current regulators; Internally lowered supply levels; Compensation for voltage drops (G11C 5/141 takes precedence)}	
M	G11C 7/00	0	Arrangements for writing information into, or reading information out from, a digital store (G11C 5/00 takes precedence; auxiliary circuits for stores using semiconductor devices G11C 11/4063, G11C 11/413)	
M	G11C 7/06	1	Sense amplifiers; Associated circuits {, e.g. timing or triggering circuits}	
M	G11C 7/1069	3	{I/O lines read out arrangements}	
M	G11C 7/20	1	Memory cell initialisation circuits, e.g. when powering up or down, memory clear, latent image memory	
M	G11C 8/00	0	Arrangements for selecting an address in a digital store (for stores using transistors G11C 11/407, G11C 11/413)	

Type*	**Symbol**	**Indent Level Number of dots (e.g. 0, 1, 2)**	**Title "CPC only" text should normally be enclosed in {curly brackets}****	**Transferred to#**
M	G11C 8/04	1	using a sequential addressing device, e.g. shift register, counter	
M	G11C 8/06	1	Address interface arrangements, e.g. address buffers	
M	G11C 8/12	1	Group selection circuits, e.g. for memory block selection, chip selection, array selection	
M	G11C 8/16	1	Multiple access memory array, e.g. addressing one storage element via at least two independent addressing line groups	
M	G11C 8/20	1	Address safety or protection circuits, i.e. arrangements for preventing unauthorized or accidental access	
M	G11C 11/02	1	using magnetic elements	
M	G11C 11/04	2	using storage elements having cylindrical form, e.g. rod, wire (G11C 11/12, G11C 11/14 take precedence)	
M	G11C 11/06035	7	{Bit core selection for writing or reading, by at least two coincident partial currents, e.g. "bit"- organised, 2L/2D, or 3D}	
M	G11C 11/06078	4	{using two or more such elements per bit}	
M	G11C 11/08	2	using multi-aperture storage elements, e.g. using transfluxors; using plates incorporating several individual multi-aperture storage elements (G11C 11/10 takes precedence)	
M	G11C 11/16	2	using elements in which the storage effect is based on magnetic spin effect	
M	G11C 11/20	2	using parametrons	
M	G11C 11/22	2	using ferroelectric elements	
M	G11C 11/23	2	using electrostatic storage on a common layer, e.g. Forrester-Haeff tubes { or William tubes}(G11C 11/22 takes precedence)	
M	G11C 11/26	2	using discharge tubes	
M	G11C 11/265	3	{counting tubes, e.g. decatrons or trochotrons}	
M	G11C 11/28	3	using gas-filled tubes	
M	G11C 11/30	3	using vacuum tubes (G11C 11/23 takes precedence)	
M	G11C 11/34	2	using semiconductor devices	
M	G11C 11/35	3	with charge storage in a depletion layer, e.g. charge coupled devices	
M	G11C 11/4072	7	Circuits for initialization, powering up or down, clearing memory or presetting	
M	G11C 11/412	5	using field-effect transistors only	
M	G11C 11/4125	6	{Cells incorporating circuit means for protecting against loss of information}	
M	G11C 11/413	5	Auxiliary circuits, e.g. for addressing, decoding, driving, writing, sensing, timing or power reduction	
M	G11C 11/42	2	using opto-electronic devices, i.e. light-emitting and photoelectric devices electrically- or optically-coupled{or feedback-coupled}	
M	G11C 11/44	2	using super-conductive elements, e.g. cryotron	

Type*	**Symbol**	**Indent Level Number of dots (e.g. 0, 1, 2)**	**Title "CPC only" text should normally be enclosed in {curly brackets}****	**Transferred to#**
M	G11C 11/50	1	using actuation of electric contacts to store the information	
M	G11C 11/56	1	using storage elements with more than two stable states represented by steps, e.g. of voltage, current, phase, frequency	
M	G11C 13/00	0	Digital stores characterised by the use of storage elements not covered by groups G11C 11/00, G11C 23/00, or G11C 25/00	
M	G11C 13/02	1	using elements whose operation depends upon chemical change {(G11C 13/0009 takes precedence)}	
M	G11C 13/04	1	using optical elements {; using other beam accessed elements, e.g. electron or ion beam}	
M	G11C 13/042	2	{using information stored in the form of interference pattern}	
M	G11C 13/06	2	using magneto-optical elements {(G11C 13/042 takes precedence)}	
M	G11C 14/00	0	Digital stores characterised by arrangements of cells having volatile and non-volatile storage properties for back-up when the power is down	
M	G11C 15/00	0	Digital stores in which information comprising one or more characteristic parts is written into the store and in which information is read-out by searching for one or more of these characteristic parts, i.e. associative or content-addressed stores	
M	G11C 16/02	1	electrically programmable	
M	G11C 16/0458	5	{comprising two or more independent floating gates which store independent data}	
M	G11C 16/0475	4	{comprising two or more independent storage sites which store independent data}	
M	G11C 16/06	2	Auxiliary circuits, e.g. for writing into memory	
M	G11C 17/00	0	Read-only memories programmable only once; Semi-permanent stores, e.g. manually-replaceable information cards	
M	G11C 17/18	2	Auxiliary circuits, e.g. for writing into memory	
M	G11C 19/00	0	Digital stores in which the information is moved stepwise, e.g. shift registers	
M	G11C 19/08	2	using thin films in plane structure	
M	G11C 19/085	3	{Generating magnetic fields therefor, e.g. uniform magnetic field for magnetic domain stabilisation}	
M	G11C 19/0866	3	{Detecting magnetic domains}	
M	G11C 19/0875	3	{Organisation of a plurality of magnetic shift registers}	
M	G11C 19/0883	4	{Means for switching magnetic domains from one path into another path, i.e. transfer switches, swap gates or decoders}	

Type*	**Symbol**	**Indent Level Number of dots (e.g. 0, 1, 2)**	**Title "CPC only" text should normally be enclosed in {curly brackets}****	**Transferred to#**
M	G11C 19/188	3	{Organisation of a multiplicity of shift registers, e.g. regeneration, timing or input-output circuits}	
M	G11C 19/28	1	using semiconductor elements (G11C 19/14, G11C 19/36 take precedence)	
M	G11C 19/287	2	{Organisation of a multiplicity of shift registers}	
M	G11C 19/30	1	using opto-electronic devices, i.e. light-emitting and photoelectric devices electrically- or optically-coupled	
M	G11C 19/32	1	using super-conductive elements	
M	G11C 19/34	1	using storage elements with more than two stable states represented by steps, e.g. of voltage, current, phase, frequency	
M	G11C 21/005	1	{using electrical delay lines}	
M	G11C 21/02	1	using electromechanical delay lines, e.g. using a mercury tank	
M	G11C 23/00	0	Digital stores characterised by movement of mechanical parts to effect storage, e.g. using balls; Storage elements therefor	
M	G11C 25/00	0	Digital stores characterised by the use of flowing media; Storage elements therefor	
M	G11C 27/00	0	Electric analogue stores, e.g. for storing instantaneous values	
M	G11C 27/02	1	Sample-and-hold arrangements (G11C 27/04 takes precedence)	
M	G11C 27/04	1	Shift registers	
M	G11C 29/00	0	Checking stores for correct operation {; Subsequent repair}; Testing stores during standby or offline operation	
M	G11C 29/006	1	{at wafer scale level, i.e. wafer scale integration [WSI]}	
M	G11C 29/48	3	Arrangements in static stores specially adapted for testing by means external to the store, e.g. using direct memory access [DMA] or using auxiliary access paths	
M	G11C 29/787	4	{using a fuse hierarchy}	
M	G11C 29/789	4	{using non-volatile cells or latches}	

*N = new entries where reclassification into entries is involved; C = entries with modified file scope where reclassification of documents from the entries is involved; Q = new entries which are firstly populated with documents via administrative transfers from deleted (D) entries. Afterwards, the transferred documents into the Q entry will either stay or be moved to more appropriate entries, as determined by intellectual reclassification; T= existing entries with enlarged file scope, which receive documents from C or D entries, e.g. when a limiting reference is removed from the entry title; M = entries with no change to the file scope (no reclassification); D = deleted entries; F = frozen entries will be deleted once reclassification of documents from the entries is completed; U = entries that are unchanged.

NOTES:

- **No {curly brackets} are used for titles in CPC only subclasses, e.g. C12Y, A23Y; 2000 series symbol titles of groups found at the end of schemes (orthogonal codes); or the Y section titles. The {curly brackets} are used for 2000 series symbol titles found interspersed throughout the main trunk schemes (breakdown codes).

- U groups: it is obligatory to display the required “anchor” symbol (U group), i.e. the entry immediately preceding a new group or an array of new groups to be created (in case new groups are not clearly subgroups of C-type groups).Always include the symbol, indent level and title of the U group in the table above.
- All entry types should be included in the scheme changes table above for better understanding of the overall scheme change picture. Symbol, indent level, and title are required for all types.
- “Transferred to” column must be completed for all C, D, F, and Q type entries. F groups will be deleted once reclassification is completed.
- When multiple symbols are included in the “Transferred to” column, avoid using ranges of symbols in order to be as precise as possible.
- For administrative transfer of documents, the following text should be used: “< administrative transfer to XX>”, “<administrative transfer to XX and YY simultaneously>”, or “<administrative transfer to XX, YY, ...and ZZ simultaneously>” when administrative transfer of the same documents is to more than one place.
- Administrative transfer to main trunk groups is assumed to be the source allocation type, unless otherwise indicated.
- Administrative transfer to 2000/Y series groups is assumed to be “additional information”.
- If needed, instructions for allocation type should be indicated within the angle brackets using the abbreviations “ADD” or “INV”: <administrative transfer to XX ADD> , <administrative transfer to XX INV>, or < administrative transfer to XX ADD, YY INV, ... and ZZ ADD simultaneously>.
- In certain situations, the “D” entries of 2000-series or Y-series groups may not require a destination (“Transferred to”) symbol, however it is required to specify “<no transfer>” in the “Transferred to” column for such cases.
- For finalisation projects, the deleted “F” symbols should have <no transfer> in the “Transferred to” column.
- For more details about the types of scheme change, see CPC Guide.

C. New, Modified or Deleted Note(s)

SUBCLASS G11C – STATIC STORES

Type*	**Location**	**Old Note**	**New/Modified Note**
M	G11C	1. This subclass covers devices or arrangements for storage of digital or analogue information in which no relative movement takes place between an information storage element and a transducer; which incorporate a selecting-device for writing-in or reading-out the information into or from the store	Replace the existing Note 1 with the following updated Note 1. 1. This subclass covers devices or arrangements for storage of digital or analogue information: • in which no relative movement takes place between an information storage element and a transducer; • which incorporate a selecting-device for writing-in or reading-out the information into or from the store.

*N = new note, M = modified note, D = deleted note

NOTE: The "Location" column only requires the symbol PRIOR to the location of the note. No further directions such as "before" or "after" are required.

2. A. DEFINITIONS (new)

Insert the following new definitions.

G11C 5/005

References

Informative References

Attention is drawn to the following places, which may be of interest for search:

Manufacturing semi-conductor by using bombardment with radiation	H01L 21/26
Error detection, monitoring	G06F 11/00

G11C 5/14

References

Informative References

Attention is drawn to the following places, which may be of interest for search:

Systems for regulating electric or magnetic variables	G05F
Circuit arrangements or systems for supplying or distributing electric power	H02J
Apparatus for conversion between AC and AC, between AC and DC or DC and DC	H02M

G11C 5/141

References

Informative References

Attention is drawn to the following places, which may be of interest for search:

Back-up supplies per se	H02J 9/061

G11C 5/142

References

Informative References

Attention is drawn to the following places, which may be of interest for search:

Circuit arrangements for transfer of electric power between ac network and dc networks	H02J 5/00

G11C 5/145

References

Limiting references

This place does not cover:

Battery and back-up supplies	G11C 5/141

Informative References

Attention is drawn to the following places, which may be of interest for search:

Charge pumps per se	H02M 3/07
For logic circuits or inverting circuits	H03K 19/00

G11C 5/146

References

Limiting references

This place does not cover:

Battery and back-up supplies	G11C 5/141

Informative References

Attention is drawn to the following places, which may be of interest for search:

Substrate bias-voltage generators	G05F 3/205

G11C 5/147

References

Limiting references

This place does not cover:

Battery and back-up supplies	G11C 5/141

Informative References

Attention is drawn to the following places, which may be of interest for search:

Regulating voltage or current using diode-transistor combinations wherein the transistors are of the field-effect type only	G05F 3/24
Regulating voltage or current wherein the variable actually regulated by the final control device as a function of the requirements of the load, temperature, specific voltage/current characteristic	G05F 1/462

G11C 7/06

References

Informative References

Attention is drawn to the following places, which may be of interest for search:

Amplifiers per se	H03F, H03K

G11C 7/1069

References

Informative References

Attention is drawn to the following places, which may be of interest for search:

Sense amplifiers; Associated circuits	G11C 7/06

G11C 8/06

References

Informative References

Attention is drawn to the following places, which may be of interest for search:

Level conversion circuits in general	H03K 19/0175

G11C 11/04

References

Informative References

Attention is drawn to the following places, which may be of interest for search:

Multi-aperture structures or multi-magnetic closed circuits, each aperture storing a "bit"	G11C 11/06085

G11C 11/08

References

Limiting references

This place does not cover:

Using multi-axial storage elements	G11C 11/10

Informative References

Attention is drawn to the following places, which may be of interest for search:

Using single-aperture storage elements; using multi-aperture plates in which each individual aperture forms a storage element	G11C 11/06

G11C 11/20

References
Informative References

Attention is drawn to the following places, which may be of interest for search:

Pulse generators using parametrons and ferroresonant devices	H03K 19/162, H03K 19/164
Counters using such elements	H03K 23/001

G11C 11/23

References

Limiting references

This place does not cover:

Using ferroelectric elements	G11C 11/22

Informative References

Attention is drawn to the following places, which may be of interest for search:

Construction of Williams tubes	H01J 31/00

G11C 11/26

References

Informative References

Attention is drawn to the following places, which may be of interest for search:

Counters using such elements	H03K 25/00

G11C 11/265

References

Informative References

Attention is drawn to the following places, which may be of interest for search:

Counters using such elements	H03K 29/00

G11C 11/28

References

Informative References

Attention is drawn to the following places, which may be of interest for search:

Counting tubes	G11C 11/265
Pulse generators, electronic switches, logic circuits using such elements	H03K 3/37, H03K 17/52, H03K 19/04

G11C 11/30

References

Informative References

Attention is drawn to the following places, which may be of interest for search:

Counting tubes	G11C 11/265
Pulse generators, electronic switches, logic circuits using such elements	H03K 3/37, H03K 17/52, H03K 19/04

G11C 11/35

References

Informative References

Attention is drawn to the following places, which may be of interest for search:

In shift registers	G11C 19/282

G11C 11/4125

References

Informative References

Attention is drawn to the following places, which may be of interest for search:

Circuit means for protection against loss of information of semiconductor storage devices in general	G11C 5/005

G11C 11/50

References

Informative References

Attention is drawn to the following places, which may be of interest for search:

Mechanical stores	G11C 23/00
Switches providing a selected number of consecutive operations of the contacts by a single manual actuation of the operating part	H01H 41/00

G11C 13/04

References

Informative References

Attention is drawn to the following places, which may be of interest for search:

Using electrostatic memory tubes	G11C 11/23
Recording of television signals	H04N 5/76

G11C 13/042

References

Informative References

Attention is drawn to the following places, which may be of interest for search:

Hologram, Lippman; Holography	G03H, G02B 5/32

G11C 16/0458

References

Informative References

Attention is drawn to the following places, which may be of interest for search:

For storage of more than two stable states at a single floating gate	G11C 11/5621

G11C 16/0475

References

Informative References

Attention is drawn to the following places, which may be of interest for search:

For storage of more than two stable states at a single floating gate	G11C 11/5621

G11C 19/08

References

Informative References

Attention is drawn to the following places, which may be of interest for search:

Thin magnetic films and apparatus or processes specially adapted for manufacturing or assembling the same	H01F 10/00, H01F 41/14

G11C 19/085

References

Informative References

Attention is drawn to the following places, which may be of interest for search:

Coil construction	H01F 5/00
Electromagnets	H01F 7/06

G11C 19/0866

References

Informative References

Attention is drawn to the following places, which may be of interest for search:

Measuring or detecting magnetic fields in general	G01R 33/02

G11C 19/0875

References

Informative References

Attention is drawn to the following places, which may be of interest for search:

Using first in first out [FIFO] registers for changing speed of digital data flow	G06F 5/06
Using last in first out [LIFO] registers for processing digital data by operating upon their order	G06F 7/78

G11C 19/0883

References

Informative References

Attention is drawn to the following places, which may be of interest for search:

Logic circuits using magnetic domains	H03K 19/168

G11C 19/188

References

Informative References

Attention is drawn to the following places, which may be of interest for search:

Using first in first out [FIFO] registers for changing speed of digital data flow	G06F 5/06
Using last in first out [LIFO] registers for processing digital data by operating upon their order	G06F 7/78

G11C 19/287

References

Informative References

Attention is drawn to the following places, which may be of interest for search:

Using first in first out [FIFO] registers for changing speed of digital data flow	G06F 5/06
Using last in first out [LIFO] registers for processing digital data by operating upon their order	G06F 7/78

G11C 19/34

References

Informative References

Attention is drawn to the following places, which may be of interest for search:

In RAM multistable cells	G11C 11/56
In capacitive analog stores	G11C 27/04

G11C 21/005

References

Informative References

Attention is drawn to the following places, which may be of interest for search:

Construction of electrical delay lines	H03H 7/30, H03H 11/26

G11C 21/02

References

Informative References

Attention is drawn to the following places, which may be of interest for search:

Construction of electromechanical delay lines	H03H 9/00

G11C 27/02

References

Informative References

Attention is drawn to the following places, which may be of interest for search:

Sampling electrical signals, in general	H03K

G11C 27/04

References

Informative References

Attention is drawn to the following places, which may be of interest for search:

Charge coupled devices per se	H01L 29/76

G11C 29/006

References

Informative References

Attention is drawn to the following places, which may be of interest for search:

For test and configuration during manufacture	H01L 22/00

G11C 29/48

References

Informative References

Attention is drawn to the following places, which may be of interest for search:

External testing equipment	G11C 29/56

2. B. DEFINITIONS QUICK FIX

Symbol	**Location of change** (e.g., section title)	**Existing reference symbol or text**	**Action; New symbol; New text**
G11C	Limiting references	Information storage based on relative movement between record carrier and transducer G11B Manufacturing processes H01L21/00, H01L45/00 Pulse technique in general, e.g. electronic switches H03K 17/00 Using a static store as a picture recording medium H04N 5/907	Delete the following references from the "Limiting references" table. Information storage based on relative movement between record carrier and transducer G11B Manufacturing processes H01L21/00, H01L45/00 Pulse technique in general, e.g. electronic switches H03K 17/00 Using a static store as a picture recording medium H04N 5/907
G11C	Limiting references	Semiconductor devices for storage; layout or structure of memory cells or devices at the fabrication level H01L 23/00, H01L 27/00, H01L 27/108 – H01L 27/115, H01L 29/00	Replace the existing reference in the "Limiting references" table with the following updated reference. Semiconductor devices for storage H01L, H01L 27/108 - H01L 27/11597
G11C	Informative references		Insert in the existing "Informative references" table, the following four new references. Information storage based on relative movement between record carrier and transducer G11B Manufacturing processes H01L21/00, H01L45/00 Pulse technique in general, e.g. electronic switches H03K 17/00

Symbol	**Location of change** (e.g., section title)	**Existing reference symbol or text**	**Action; New symbol; New text**
			Using a static store as a picture recording medium H04N 5/907
G11C 5/00	Limiting references	Power supplies, reference generators or voltage pumps in general not being concerned with semiconductor memories. G05F, H02J, H02M Circuit means for protection against loss of information in general having no connection to semiconductor memories. H01L 21/26, G06F 11/00 Geometrical lay-out of the components in integrated circuits not concerned with semiconductor memories H01L 27/0207 Mechanical aspects of memory modules, supports and cards H05K 5/02, H01L 25/00	Delete the entire "Limiting references" section.
G11C 5/00	Application-oriented references	Means for protection concerning static memory storage device (SRAM) G11C 11/41355 Power supply arrangements for SRAMs G11C 11/41357	Delete from the "Application-oriented references" table the following two references. Means for protection concerning static memory storage device (SRAM) G11C 11/41355 Power supply arrangements for SRAMs G11C 11/41357

Symbol	**Location of change** (e.g., section title)	**Existing reference symbol or text**	**Action; New symbol; New text**
G11C 5/00	Informative references		Insert the following new "Informative references" section. **Informative references** *Attention is drawn to the following places, which may be of interest for search:* Power supplies, reference generators or voltage pumps in general not being concerned with semiconductor memories G05F, H02J, H02M Circuit means for protection against loss of information in general having no connection to semiconductor memories H01L 21/26, G06F 11/00 Geometrical lay-out of the components in integrated circuits not concerned with semiconductor memories H01L 27/0207 Mechanical aspects of memory modules, supports and cards H05K 5/02, H01L 25/00
G11C 5/143	Limiting references	Testing of electric apparatus, lines or components, for short-circuits, discontinuities, leakage G01R 31/50 Back-up supplies per se H02J 9/061	Delete the following two references from the "Limiting references" table. Testing of electric apparatus, lines or components, for short-circuits, discontinuities, leakage G01R 31/50 Back-up supplies per se H02J 9/061

Symbol	**Location of change** (e.g., section title)	**Existing reference symbol or text**	**Action; New symbol; New text**
G11C 5/143	Informative references		Insert the following new "Informative references" section. **Informative references** *Attention is drawn to the following places, which may be of interest for search:* Testing of electric apparatus, lines or components, for short-circuits, discontinuities, leakage G01R 31/50 Back-up supplies per se H02J 9/061
G11C 7/00	Limiting references	Specific cell types of technologies G11C 11/00, G11C 17/00 Higher level memory space management, free space management, garbage collection, cache memories G06F12/00 External memory control circuits, buses, bus protocols, DMA, memory controllers G06F 13/16 Encryption, data protection G06F2211/007, G06F 12/00	Delete the following references from the "Limiting references" table. Specific cell types of technologies G11C 11/00, G11C 17/00 Higher level memory space management, free space management, garbage collection, cache memories G06F 12/00 External memory control circuits, buses, bus protocols, DMA, memory controllers G06F 13/16 Encryption, data protection G06F 2211/007, G06F 12/00
G11C 7/00	Application-oriented references	Reading and writing arrangements for specific cell types G11C 11/00 – G11C 17/00	Replace the existing reference with the following updated reference. Reading and writing arrangements for specific cell types G11C 17/00

Symbol	**Location of change** (e.g., section title)	**Existing reference symbol or text**	**Action; New symbol; New text**
G11C 7/00	Informative references		Remove the reference symbol G06F 13/16 corresponding to "Calibration"
G11C 7/00	Informative references		Insert the following new references in the existing “Informative references” table. Higher level memory space management, free space management, garbage collection, cache memories G06F 12/00
G11C 8/00	Limiting references	Shift registers in general, FIFO, LIFO G11C 19/08, G06F 5/06 Addressing schemes, architectures or methods, e.g. virtual addressing or multidimensional addressing G06F 12/00 Address mapping G06F 12/02 Switching or gating circuits for general use H03K 17/00 Encoding or decoding method per se H03M 7/00	Delete the following existing references from the “Limiting references” table. Shift registers in general, FIFO, LIFO G11C 19/08, G06F 5/06 Addressing schemes, architectures or methods, e.g. virtual addressing or multidimensional addressing G06F 12/00 Address mapping G06F 12/02 Switching or gating circuits for general use H03K 17/00 Encoding or decoding method per se H03M 7/00

Symbol	**Location of change** (e.g., section title)	**Existing reference symbol or text**	**Action; New symbol; New text**
G11C 8/00	Limiting references		Insert the following new reference in the existing "Limiting references" table. Digital stores characterised by the use of particular electric or magnetic storage elements G11C 11/00
G11C 8/00	Application-oriented references	Particular aspects concerning addressing SRAM (static RAM) devices G11C 11/41313	Delete from the "Application-oriented references" table the following existing reference. Particular aspects concerning addressing SRAM (static RAM) devices G11C 11/41313
G11C 8/00	Informative references		Insert the following new "Informative references" section. **Informative references** *Attention is drawn to the following places, which may be of interest for search:* Shift registers in general, FIFO, LIFO G11C 19/08, G06F 5/06 Addressing schemes, architectures or methods, e.g. virtual addressing or multidimensional addressing G06F 12/00 Address mapping G06F 12/02 Switching or gating circuits for general use H03K 17/00 Encoding or decoding method per se H03M 7/00

Symbol	**Location of change** (e.g., section title)	**Existing reference symbol or text**	**Action; New symbol; New text**
G11C 8/04	Limiting references		Delete the entire existing “Limiting references” section.
G11C 8/04	Informative references		Insert in the existing “Informative references” table the following new references. Using first in first out [FIFO] registers for changing speed of digital data flow G06F 5/06 Using last in first out [LIFO] registers for processing digital data by operating upon their order G06F 7/00
G11C 8/16	Limiting references		Delete the entire existing “Limiting references” section.
G11C 8/16	Informative references		Insert the following new “Informative references” section. **Informative references** *Attention is drawn to the following places, which may be of interest for search:* Multiport memories in general G11C 7/1075
G11C 11/00	Definition statement	• DRAM (Dynamic RAM), see G11C 11/401 - G11C 11/4099 • FRAM, FeRAM (Ferro-electric RAM) see G11C 11/22 • MRAM (Magnetic RAM) see G11C 11/14 - G11C 11/16	Replace in the existing “Definition statement” section the first four statements with updated text as shown below. • DRAM [Dynamic RAM], see G11C 11/401 - G11C 11/4099 • FRAM, FeRAM [Ferro-electric RAM] see G11C 11/22

Symbol	**Location of change** (e.g., section title)	**Existing reference symbol or text**	**Action; New symbol; New text**
		• SRAM (Static RAM) see G11C 11/41 - G11C 11/419	• MRAM [Magnetic RAM] see G11C 11/14 - G11C 11/16 • SRAM [Static RAM] see G11C 11/41 - G11C 11/419
G11C 11/00	Limiting references	General aspects of power supplies, charge pumps, voltage references and battery backup G11C 5/00 NVRAM Nonvolatile battery backed up RAM G11C 5/41 General aspects of input/output selection, read and write circuitry. G11C 7/00 General aspects of address decoding and word line selection. G11C 8/00 RRAM, ReRAM (Resistive RAM) G11C 13/0002 – G11C 13/0097 PCRAM, PRAM (Phase-change RAM) G11C 13/0004 General aspects of testing G11C 29/00 General aspects of redundancy management G11C 29/70	Delete the following eight references from the existing "Limiting references" table. General aspects of power supplies, charge pumps, voltage references and battery backup G11C 5/00 NVRAM Nonvolatile battery backed up RAM G11C 5/141 General aspects of input/output selection, read and write circuitry. G11C 7/00 General aspects of address decoding and word line selection. G11C 8/00 RRAM, ReRAM (Resistive RAM) G11C 13/0002 – G11C 13/0097 PCRAM, PRAM (Phase-change RAM) G11C 13/0004 General aspects of testing G11C 29/00 General aspects of redundancy management G11C 29/70

Symbol	**Location of change** (e.g., section title)	**Existing reference symbol or text**	**Action; New symbol; New text**
G11C 11/00	Informative references		Insert in the existing "Informative references" table the following new references. General aspects of power supplies, charge pumps, voltage references and battery backup G11C 5/00 NVRAM [Nonvolatile RAM] battery backed up RAM G11C 5/141 General aspects of input/output selection, read and write circuitry G11C 7/00 General aspects of address decoding and word line selection G11C 8/00 RRAM, ReRAM [Resistive RAM] G11C 13/0002 – G11C 13/0097 PCRAM, PRAM [Phase-change RAM] G11C 13/0004 General aspects of testing G11C 29/00 General aspects of redundancy management G11C 29/70
G11C 11/16	Limiting references		Delete the entire "Limiting references" section.
G11C 11/16	Informative references		Insert in the existing "Informative references" table the following new references. Sensors using magnetoresistance multilayer structures G01R 33/093 Thin layer magnetic read heads for magnetic discs G11B 5/31

Symbol	**Location of change** (e.g., section title)	**Existing reference symbol or text**	**Action; New symbol; New text**
			Composition of ferromagnetic material H01F 1/00 Non-reciprocal magnetic elements in waveguides H01P Gyrators H03H 7/002
G11C 11/22	Limiting references		Delete the entire existing “Limiting references” section.
G11C 11/22	Informative references		Insert in the existing “Informative references” table the following three new references. Using multibit ferroelectric storage G11C 11/5657 Pulse generators using ferroelectric elements H03K 3/45 Counters using such elements H03K 23/76
G11C 11/56	Informative references		Insert the following new “Informative references” section. **Informative references** *Attention is drawn to the following places, which may be of interest for search:* Counting arrangements comprising multi-stable elements of this type H03K 25/00, H03K 29/00
G11C 13/00	Limiting references	Digital stores in which the storage effect is based exclusively on magnetism e.g. Magnetic RAM (MRAM) G11C 11/15,	Replace the existing reference in the “Limiting references” table with the following updated reference. Digital stores in which the storage effect is based exclusively on

Symbol	**Location of change** (e.g., section title)	**Existing reference symbol or text**	**Action; New symbol; New text**
		G11C 11/16	magnetism e.g. Magnetic RAM (MRAM) G11C 11/00, G11C 23/00, G11C 25/00
G11C 13/02	Limiting references	Using electrochemical charge G11C 11/00	Replace the existing reference in the "Limiting references" table with the following updated reference. RRAM elements whose operation depends upon chemical change G11C 13/0009
G11C 13/02	Informative references		Insert the following new "Informative references" section. **Informative references** *Attention is drawn to the following places, which may be of interest for search:* Using electrochemical charge G11C 11/00
G11C 13/06	Limiting references	Using magnetic-optical storage elements G11C 13/043	Delete the following row from the existing "Limiting references" table. Using magnetic-optical storage elements G11C 13/043
G11C 13/06	Informative references		Insert in the existing "Informative references" table the following new reference. Using magnetic-optical storage elements G11C 13/043
G11C 14/00	Limiting references		Delete the entire "Limiting references" section.

Symbol	**Location of change** (e.g., section title)	**Existing reference symbol or text**	**Action; New symbol; New text**
G11C 14/00	Informative references		Insert the following new "Informative references" section. **Informative references** *Attention is drawn to the following places, which may be of interest for search:* Bistable elements storing the actual state when the supply voltage fails H03K 3/02335, H03K 3/0375, H03K 3/2865 H03K 3/356008
G11C 15/00	Limiting references	References Limiting references *This place does not cover:* Digital stores in which information is addressed to a specific location G11C 11/00 Selection information using addressing means, e.g. hashing, tree addressing, chaining G06F 11/22 Information retrieval systems using a computer G06F 16/00	Delete the entire "Limiting references" section.
G11C 15/00	Informative references		Insert the following new "Informative references" section. **Informative references** *Attention is drawn to the following places, which may be of interest for search:* Digital stores in which information is addressed to a specific location G11C 11/00

Symbol	**Location of change** (e.g., section title)	**Existing reference symbol or text**	**Action; New symbol; New text**
			Selection information using addressing means, e.g. hashing, tree addressing, chaining G06F 11/22 Information retrieval systems using a computer G06F 16/00
G11C 16/00	Limiting references	NVRAM Nonvolatile battery backed up RAM G11C 5/141 Digital stores in which the storage effect is based exclusively on magnetism e.g. Magnetic RAM (MRAM) G11C 11/15, G11C 11/16 FeRAMs G11C 11/22 RRAM, ReRAM (Resistive RAM) G11C 13/0002 - G11C 13/0097 PCRAM, PRAM (Phase-change RAM) G11C 13/0004 Fabrication of EPROM H01L 27/115 EPROM memory structures H01L 27/115	Delete from the Limiting references table the following references. NVRAM Nonvolatile battery backed up RAM G11C 5/141 Digital stores in which the storage effect is based exclusively on magnetism e.g. Magnetic RAM (MRAM) G11C 11/15, G11C 11/16 FeRAMs G11C 11/22 RRAM, ReRAM (Resistive RAM) G11C 13/0002 - G11C 13/0097 PCRAM, PRAM (Phase-change RAM) G11C 13/0004 Fabrication of EPROM H01L 27/115 EPROM memory structures H01L 27/115
G11C 16/00	Application-oriented references		Delete the entire Application-oriented references section.
G11C 16/00	Informative references		Insert the following new references in the existing Informative references table.

Symbol	**Location of change** (e.g., section title)	**Existing reference symbol or text**	**Action; New symbol; New text**
			NVRAM Nonvolatile battery backed up RAM G11C 5/141 Digital stores in which the storage effect is based exclusively on magnetism e.g. Magnetic RAM (MRAM) G11C 11/15, G11C 11/16 FeRAMs G11C 11/22 RRAM, ReRAM (Resistive RAM) G11C 13/0002 - G11C 13/0097 PCRAM, PRAM (Phase-change RAM) G11C 13/0004 Fabrication of EPROM H01L 27/115 EPROM memory structures H01L 27/115
G11C 17/00	Limiting references	Limiting references *This place does not cover:* Multibit read only memories G11C 11/5692 Rewritable resistive memories (RRAM) G11C 13/0002 Erasable programmable read-only memories G11C 16/00 Fabrication of read only memories H01L 21/8246 Read only memory structures H01L 27/112	Delete the entire “Limiting references” section.

Symbol	**Location of change** (e.g., section title)	**Existing reference symbol or text**	**Action; New symbol; New text**
G11C 17/00	Informative references		Insert the following new "Informative references" section. **Informative references** *Attention is drawn to the following places, which may be of interest for search:* Multibit read only memories G11C 11/5692 Rewritable resistive memories (RRAM) G11C 13/0002 Erasable programmable read-only memories G11C 16/00 Read only memory structures H01L 27/112 Coding, decoding or code conversion, in general H03M
G11C 19/00	Limiting references	Limiting references *This place does not cover:* Methods and arrangements for shifting data G06F 5/01 Pulse distributors H03K 5/15 Counting chains H03K 23/00 Linear pulse counters H03K 23/54	Delete the entire "Limiting references" section.
G11C 19/00	Informative references		Insert the following new "Informative references" section. **Informative references** *Attention is drawn to the following places, which may be of interest for search:*

Symbol	**Location of change** (e.g., section title)	**Existing reference symbol or text**	**Action; New symbol; New text**
			Method and arrangements for shifting data G06F 5/01 Pulse distributors H03K 5/15 Counting chains H03K 23/00 Linear pulse counters H03K 23/54
G11C 23/00	Limiting references	**References** **Limiting references** *This place does not cover*: Storing by actuating contacts G11C 11/50	Delete the entire "Limiting references" section.
G11C 23/00	Informative references		Insert in the existing "Informative references" table the following new reference. Storing by actuating contacts G11C 11/50
G11C 25/00	Limiting references	**References** **Limiting references** *This place does not cover:* Multiple fluid-circuit element arrangements for performing digital Operations F15C 1/12	Delete the entire "Limiting references" section.
G11C 25/00	Informative references		Insert the following new "Informative references" section. **Informative references** *Attention is drawn to the following places, which may be of interest for search:* Multiple fluid-circuit element arrangements for performing digital operations F15C 1/12

Symbol	**Location of change** (e.g., section title)	**Existing reference symbol or text**	**Action; New symbol; New text**
G11C 27/00	Limiting references	References Limiting references *This place does not cover:* Integrating circuits acting as stores G06G 7/18 Pulse counters with step by step integration and static storage H03K 25/00	Delete the entire "Limiting references" section.
G11C 27/00	Informative references		Insert in the "Informative references" table, the following two new references. Integrating circuits acting as stores G06G 7/18 Pulse counters with step by step integration H03K 25/00
G11C 29/00	Limiting references		Delete the entire "Limiting references" section.
G11C 29/00	Informative references		Insert in the existing "Informative references" table the following three new references. Test of electronic circuits in general G01R 31/28 Testing of computers during standby G06F 11/22
G11C 29/00	Special rules of classification	G11C 29/56: tester apparatus features G11C29/66 Test of serial memories e.g. FIFO, stacks serial buffers G11C29/68 Testing at wafer scale level e.g. features particular related to wafer test, probing, test	Replace in the existing text in the "Special rules of classification" section with the following statements. G11C 29/56: tester apparatus features

Symbol	**Location of change** (e.g., section title)	**Existing reference symbol or text**	**Action; New symbol; New text**
		circuit location on wafer, e.g. in cut slot, chip identification, IDDQ-test. For test and configuration during manufacturing, see H01L21/66.	

NOTES:

- The table above is used for corrections or modifications to existing definitions, e.g. delete an entire definition or part thereof; propose new wording or modify wording of a section, change the symbol the definition is associated with, change or delete a reference symbol, etc.
- Do not delete (F) symbol definitions.